FCRP Memory Cross-Cut Workshop

Thursday May 12, 2011

Massachusetts Institute of Technology - Cambridge, MA

Registration via Joint FENA/MSD Annual Review

https://www-mtl.mit.edu/MSD/

Time	Topic	Speaker
7:30-8:00	Registration and Breakfast	
8:00-8:15	Welcome and Overview	H.-S. Philip Wong, Stanford
8:15-9:30	Session 1: System Level Memory Challenges	Chair: David Brooks, Harvard
8:15-8:40	Fixing the Memory Power Problem	Chris Wilkerson, Intel
8:40-9:05	Architecture and System-Level Challenges in Multi-Core Memory Systems	Onur Mutlu, CMU
9:05-9:30	Architecting Main Memories with Storage Class Memories	Moinuddin Qureshi, IBM
9:30-9:55	Session 1 Panel	
9:55-10:20	Break	
10:20-11:35	Session 2: Device Opportunities and Circuit/System Needs	Chair: Leland Chang, IBM
10:20-10:45	The Alphabet Soup of Emerging Memory Devices	H.-S. Philip Wong, Stanford
10:45-11:10	Emerging Memory Challenges and Requirements	Gurtej Sandhu, Micron
11:10-11:35	Memory Cell Selection Device Challenges	Kaliash Gopalakrishnan, IBM
11:35-11:50	A Universal SPICE Model of Memory Devices	Kevin Cao, ASU
11:50-12:15	Session 2 Panel	
12:15-1:15	Lunch	
1:15-2:30	Session 3: Non-Volatile Nano-Memory	Chair: Steve Kramer, Micron
1:15-1:40	Wide Band Gap Emerging Memory	Jianlin Liu, UC Riverside
1:40-2:05	Is STTRAM the universal memory?	Sanjay Banerjee, UT Austin
2:05-2:30	Notes from the Far Side: Unconventional Thoughts for Nanoscale	Sandip Tiwari, Cornell
2:30-3:00	Session 3 Panel	